DEVICES INCORPORATED

LF2246

11 x 10-bit Image Filter

FEATURES

- 66 MHz Data and Coefficient Input and Computation Rate
- Four 11 x 10-bit Multipliers with Individual Data and Coefficient Inputs and a 25-bit Accumulator
- User-Selectable Fractional or Integer Two's Complement Data Formats
- Fully Registered, Pipelined Architecture
- Input and Output Data Registers, with User-Configurable Enables
- Three-State Outputs
- Fully TTL Compatible
- Ideally Suited for Image Processing and Filtering Applications
- Replaces TRW/Raytheon/Fairchild TMC2246
- 120-pin PQFPP

DESCRIPTION

The **LF2246** consists of an array of four 11 x 10-bit registered multipliers followed by a summer and a 25-bit accumulator. All multiplier inputs are user accessible and can be updated every clock cycle with either fractional or integer two's complement data. The pipelined architecture has fully registered input and output ports and an asynchronous three-state output enable control to simplify the design of complex systems. The pipeline latency for all inputs is five clock cycles.

Storage for mixing and filtering coefficients can be accomplished by holding the data or coefficient inputs over multiple clock cycles. A 25-bit accumulator path allows cumulative word growth which may be internally rounded to 16 bits. Output data is updated every clock cycle and may be held under user control. All inputs, outputs, and controls are registered on the rising edge of clock, except for $\overline{OEN}$. The LF2246 operates at a clock rate of 66 MHz over the full temperature and supply voltage ranges.

The LF2246 is applicable for performing pixel interpolation in image manipulation and filtering applications. The LF2246 can perform a bilinear interpolation of an image (4-pixel kernels) at real-time video rates when used with an image resampling sequencer. Larger kernels or more complex functions can be realized by utilizing multiple devices.

Unrestricted access to all data and coefficient input ports provides the LF2246 with considerable flexibility in applications such as digital filters, adaptive FIR filters, mixers, and other similar systems requiring high-speed processing.

LF2246 Block Diagram

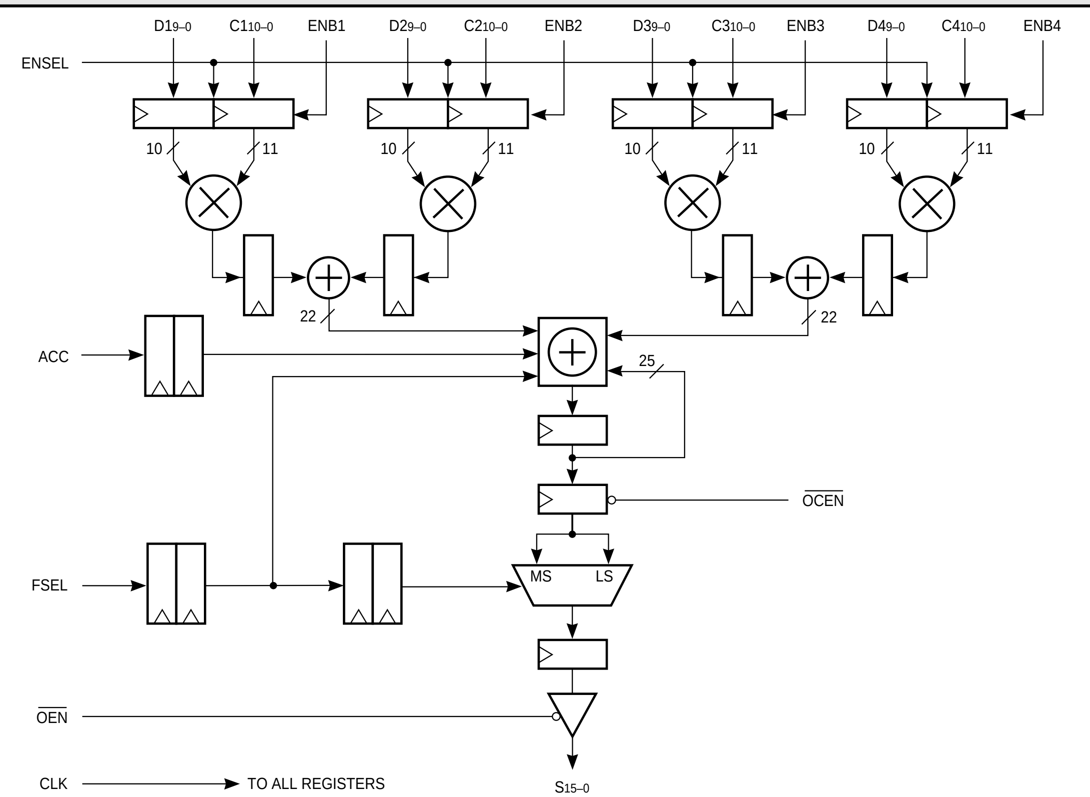


FIGURE 1A. INPUT FORMATS

Data

Fractional Two's Complement (FSEL = 0)

9	8	7		2	1	0
-2^{0} (Sign)	2^{-1}	2^{-2}		2^{-7}	2^{-8}	2^{-9}

Integer Two's Complement (FSEL = 1)

9	8	7		2	1	0
-2^{9} (Sign)	2^{8}	2^{7}		2^{2}	2^{1}	2^{0}

Coefficient

Fractional Two's Complement (FSEL = 0)

10	9	8		2	1	0
-2^{1} (Sign)	2^{0}	2^{-1}		2^{-7}	2^{-8}	2^{-9}

Integer Two's Complement (FSEL = 1)

10	9	8		2	1	0
-2^{10} (Sign)	2^{9}	2^{8}		2^{2}	2^{1}	2^{0}

FIGURE 1B. OUTPUT FORMATS

Fractional Two's Complement (FSEL = 0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{6} (Sign)	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

Integer Two's Complement (FSEL = 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{15} (Sign)	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

D1$_{9-0}$–D4$_{9-0}$ — Data Input

D1–D4 are 10-bit data input registers. The LSB is DN0 (Figure 1a).

C1$_{10-0}$–C4$_{10-0}$ — Coefficient Input

C1–C4 are 11-bit coefficient input registers. The LSB is CN0 (Figure 1a).

Outputs

S$_{15-0}$ — Data Output

The current 16-bit result is available on the S$_{15-0}$ outputs (Figure 1b).

Controls

ENB1–ENB4 — Input Enable

The ENBN (N = 1, 2, 3, or 4) input allows either or both the DN and CN registers to be updated on each clock cycle. When ENBN is LOW, registers DN and CN are both strobed by the next rising edge of CLK. When ENBN is HIGH and ENSEL is LOW, register DN is strobed while register CN is held. If both ENBN and ENSEL are HIGH, register DN is held, and register CN is strobed (Table 1).

ENSEL — Enable Select

The ENSEL input in conjunction with the individual input enables ENB1–ENB4 determines whether the data or the coefficient input registers will be held on the next rising edge of CLK (Table 1).

$\overline{\text{OEN}}$ — Output Enable

When the $\overline{\text{OEN}}$ signal is LOW, the current data in the output register is available on the S$_{15-0}$ pins. When $\overline{\text{OEN}}$ is HIGH, the outputs are in a high-impedance state.

TABLE 1. INPUT REGISTER CONTROL

ENB1-4	ENSEL	INPUT REGISTER HELD
1	1	Data 'N'
1	0	Coefficient 'N'
0	X	None

X = "Don't Care"
'N' = 1, 2, 3, or 4

$\overline{\text{OCEN}}$ — Clock Enable

When $\overline{\text{OCEN}}$ is LOW, data in the pre-mux register (accumulator output) is loaded into the output register on the next rising edge of CLK. When $\overline{\text{OCEN}}$ is HIGH, data in the pre-mux register is held preventing the output register's contents from changing (if FSEL does not change). Accumulation continues internally as long as ACC is HIGH, despite the state of $\overline{\text{OCEN}}$.

FSEL — Format Select

When the FSEL input is LOW, the data input during the current clock cycle is assumed to be in fractional two's complement format, and the upper 16 bits of the accumulator are presented at the output. Rounding of the accumulator result to 16 bits is performed if the accumulator control input ACC is LOW. When FSEL is HIGH, the data input is assumed to be in integer two's complement format, and the lower 16 bits of the accumulator are presented at the output. No rounding is performed when FSEL is HIGH.

ACC — Accumulator Control

The ACC input determines whether internal accumulation is performed on the data input during the current clock cycle. If ACC is LOW, no accumulation is performed, the prior accumulated sum is cleared, and the current sum of products is output. If FSEL is also LOW, one-half LSB rounding to 16 bits is performed on the result. This allows summations without propagating roundoff errors. When ACC is HIGH, the emerging product is added to the sum of the previous products, without additional rounding.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature .... –65°C to +150°C
Operating ambient temperature .... –55°C to +125°C
V_{CC} supply voltage with respect to ground .... –0.5 V to +7.0 V
Input signal with respect to ground .... –0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output .... –0.5 V to V_{CC} + 0.5 V
Output current into low outputs .... 25 mA
Latchup current .... > 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	(Note 12)			±40	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			100	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			6	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

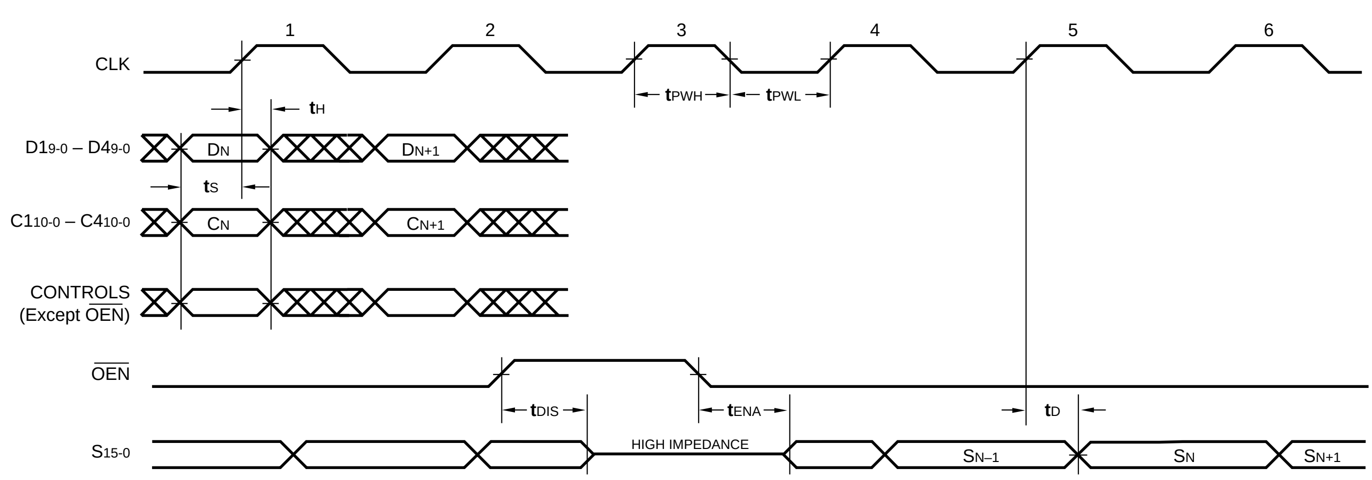
Commercial Operating Range (0°C to +70°C) *Notes 9, 10 (ns)*

		LF2246–					
		33*		25		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	33		25		15	
t_{PWL}	Clock Pulse Width Low	15		10		7	
t_{PWH}	Clock Pulse Width High	10		10		7	
t_S	Input Setup Time	10		8		5	
t_H	Input Hold Time	0		0		0	
t_D	Output Delay		15		13		11
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		15		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15		15

Military Operating Range (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF2246–			
		33*		25*	
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Cycle Time	33		25	
t_{PWL}	Clock Pulse Width Low	15		10	
t_{PWH}	Clock Pulse Width High	10		10	
t_S	Input Setup Time	10		8	
t_H	Input Hold Time	0		0	
t_D	Output Delay		15		13
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15

Switching Waveforms



*Discontinued Speed Grade

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 30 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

Figure A. Output Loading Circuit

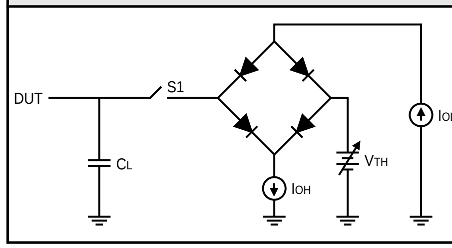
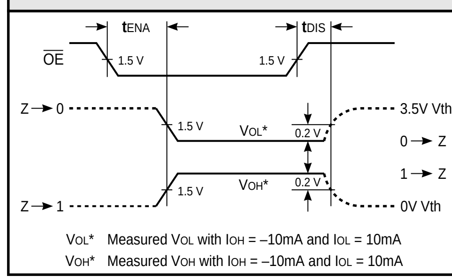
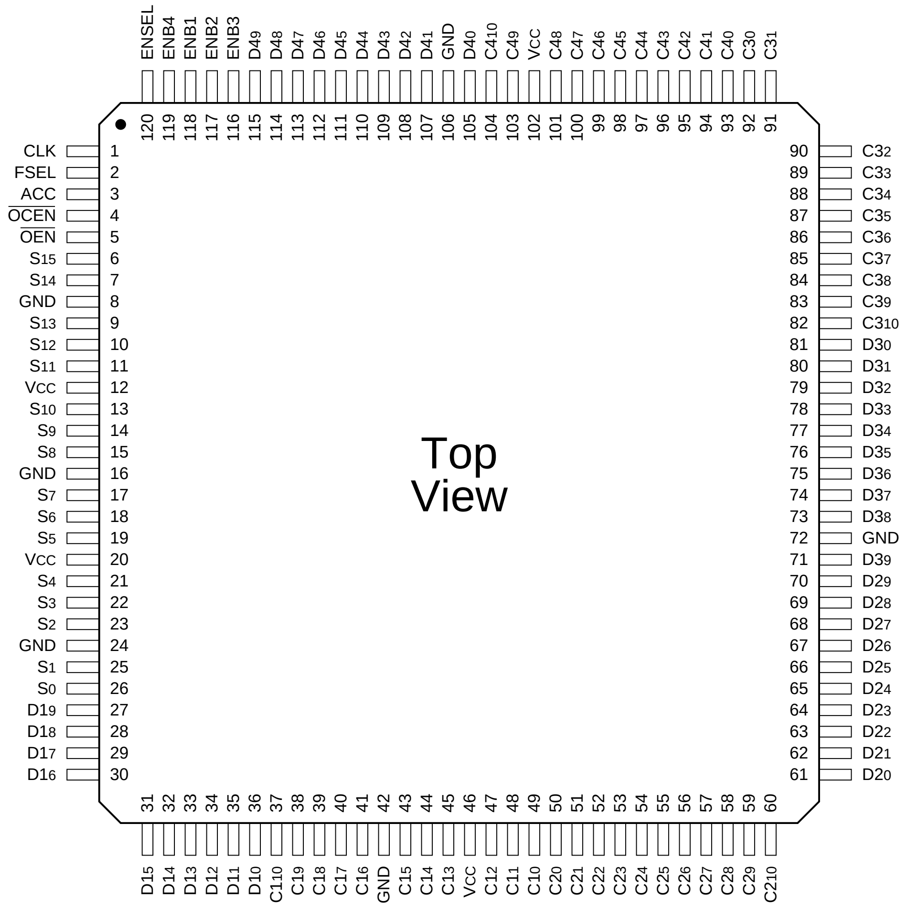


Figure B. Threshold Levels



ORDERING INFORMATION

120-pin



Speed	Plastic Quad Flatpack (Q1)
	0°C to +70°C — Commercial Screening
25 ns	LF2246QC25
15 ns	LF2246QC15
	–40°C to +85°C — Commercial Screening

ORDERING INFORMATION

120-pin

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	ENSEL	ENB2	ENB3	$D4_7$	$D4_5$	$D4_2$	$D4_1$	$C4_{10}$	$C4_8$	$C4_6$	$C4_3$	$C4_0$	$C3_2$
B	ACC	FSEL	ENB4	$D4_9$	$D4_6$	$D4_3$	$D4_0$	$C4_9$	$C4_7$	$C4_4$	$C4_2$	$C3_0$	$C3_5$
C	S_{15}	$\overline{\text{OEN}}$	CLK	ENB1	$D4_8$	$D4_4$	GND	V_{CC}	$C4_5$	$C4_1$	$C3_1$	$C3_3$	$C3_6$
D	S_{13}	S_{14}	$\overline{\text{OCEN}}$								$C3_4$	$C3_7$	$C3_9$
E	S_{11}	S_{12}	GND								$C3_8$	$C3_{10}$	$D3_0$
F	S_9	S_{10}	V_{CC}								$D3_1$	$D3_2$	$D3_3$
G	S_7	S_8	GND								$D3_5$	$D3_6$	$D3_4$
H	S_6	S_5	V_{CC}								GND	$D3_8$	$D3_7$
J	S_4	S_3	GND								$D2_7$	$D2_9$	$D3_9$
K	S_2	S_1	$D1_8$								$D2_3$	$D2_6$	$D2_8$
L	S_0	$D1_7$	$D1_5$	$D1_2$	$C1_9$	GND	V_{CC}	$C2_0$	$C2_4$	$C2_8$	$D2_0$	$D2_4$	$D2_5$
M	$D1_9$	$D1_4$	$D1_1$	$C1_{10}$	$C1_7$	$C1_5$	$C1_3$	$C1_0$	$C2_2$	$C2_5$	$C2_9$	$D2_1$	$D2_2$
N	$D1_6$	$D1_3$	$D1_0$	$C1_8$	$C1_6$	$C1_4$	$C1_2$	$C1_1$	$C2_1$	$C2_3$	$C2_6$	$C2_7$	$C2_{10}$

KEY

Top View
Through Package
(i.e., Component Side Pinout)

Discontinued Package

Speed	Ceramic Pin Grid Array (G4)
	0°C to +70°C — COMMERCIAL SCREENING
	–40°C to +80°C — COMMERCIAL SCREENING
	–55°C to +125°C — MIL-STD-883 COMPLIANT